

FIG. 1

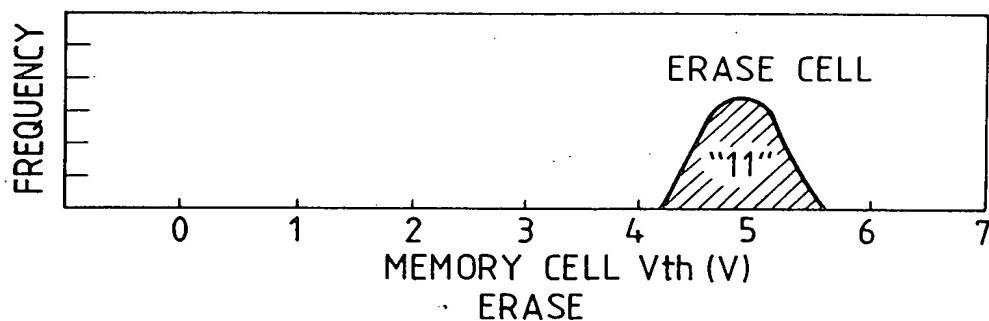
(1)	1ST DATA a	0	1	0	1
	1ST DATA b	0	0	1	1
	2-BIT DATA	'00'	'01'	'10'	'11'
(2)	1ST OPERATION (a NAND b)	1	1	1	0
	2ND OPERATION (NOT b)	1	1	0	0
	3RD OPERATION (a NOR b)	1	0	0	0
	NO. OF 1	3	2	1	0
(3)	DATA	THRESHOLD VALUE			
	'00'	V ₀ - 3V _a			
	'01'	V ₀ - 2V _a			
	'10'	V ₀ - V _a			
	'11'	V ₀ (=ERASE LEVEL)			

FIG. 2

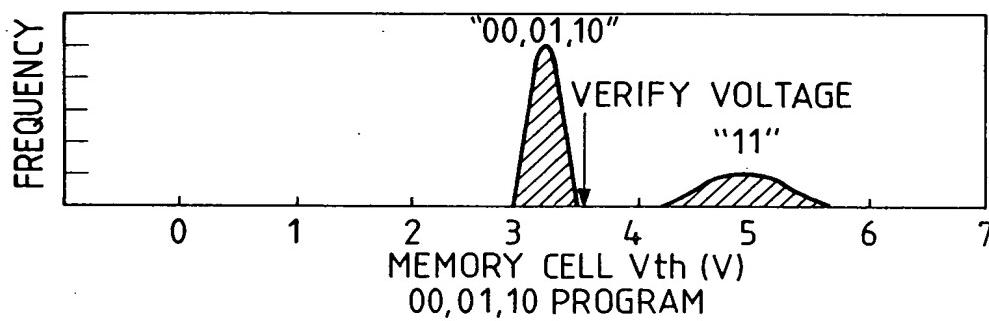
c	0	0	0	1	(READ LEVEL: HIGH)
d	0	0	1	1	(READ LEVEL: MEDIUM)
f	0	1	1	1	(READ LEVEL: LOW)
\bar{d} NAND f	1	0	1	1	
(\bar{d}) NAND f) NAND \bar{c}	0	1	0	1	= a
d	0	0	1	1	= b

FIG. 3

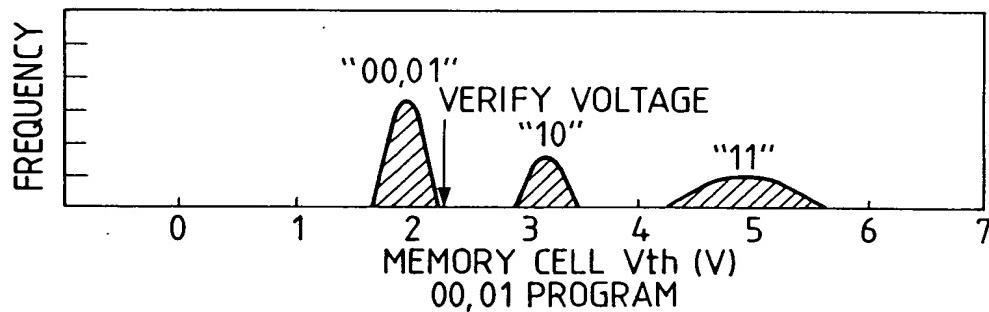
(1)



(2)



(3)



(4)

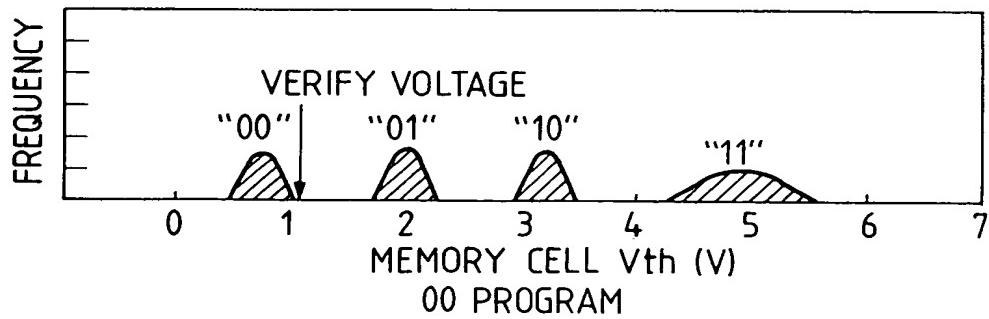


FIG. 4

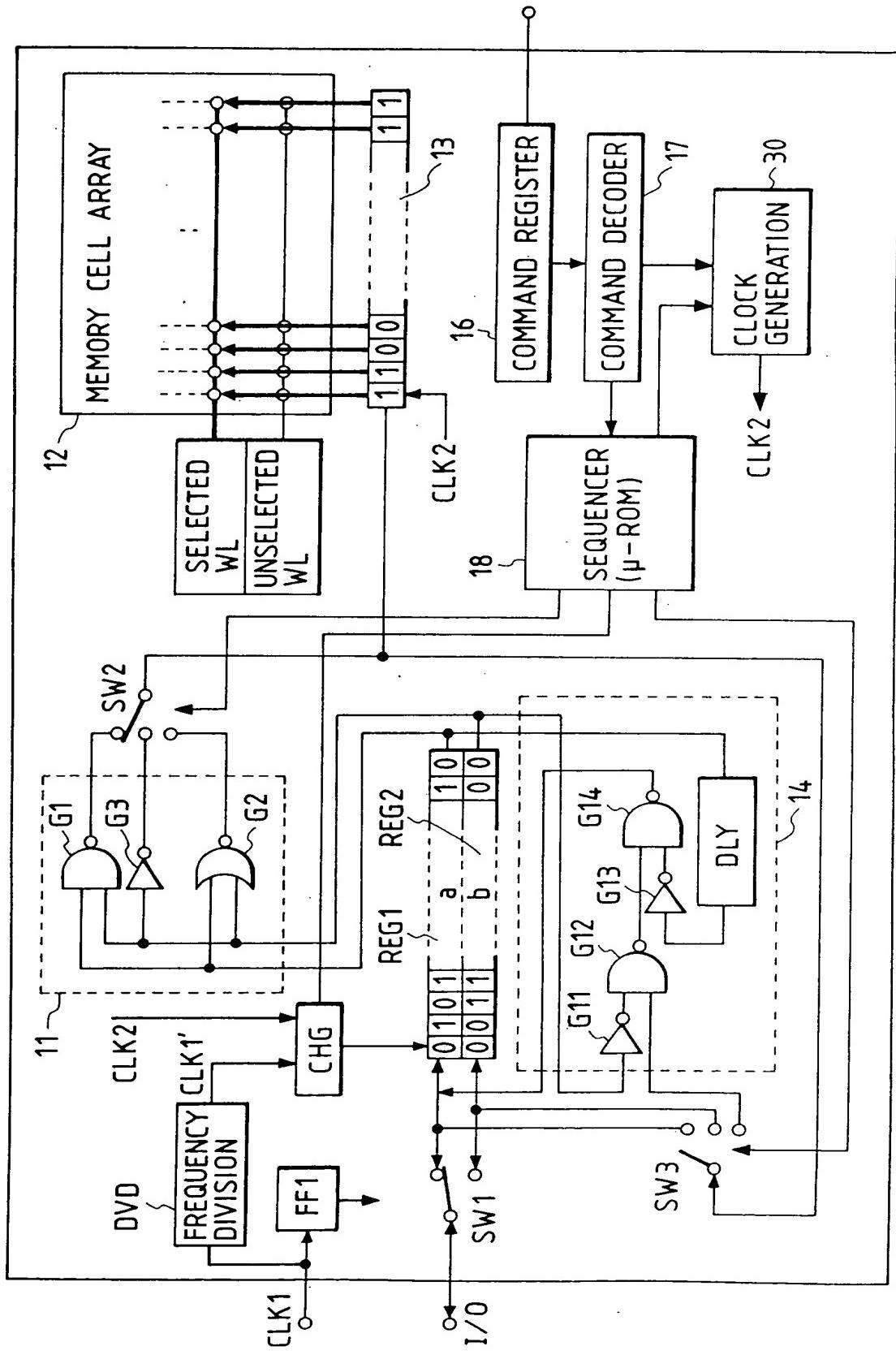


FIG. 5

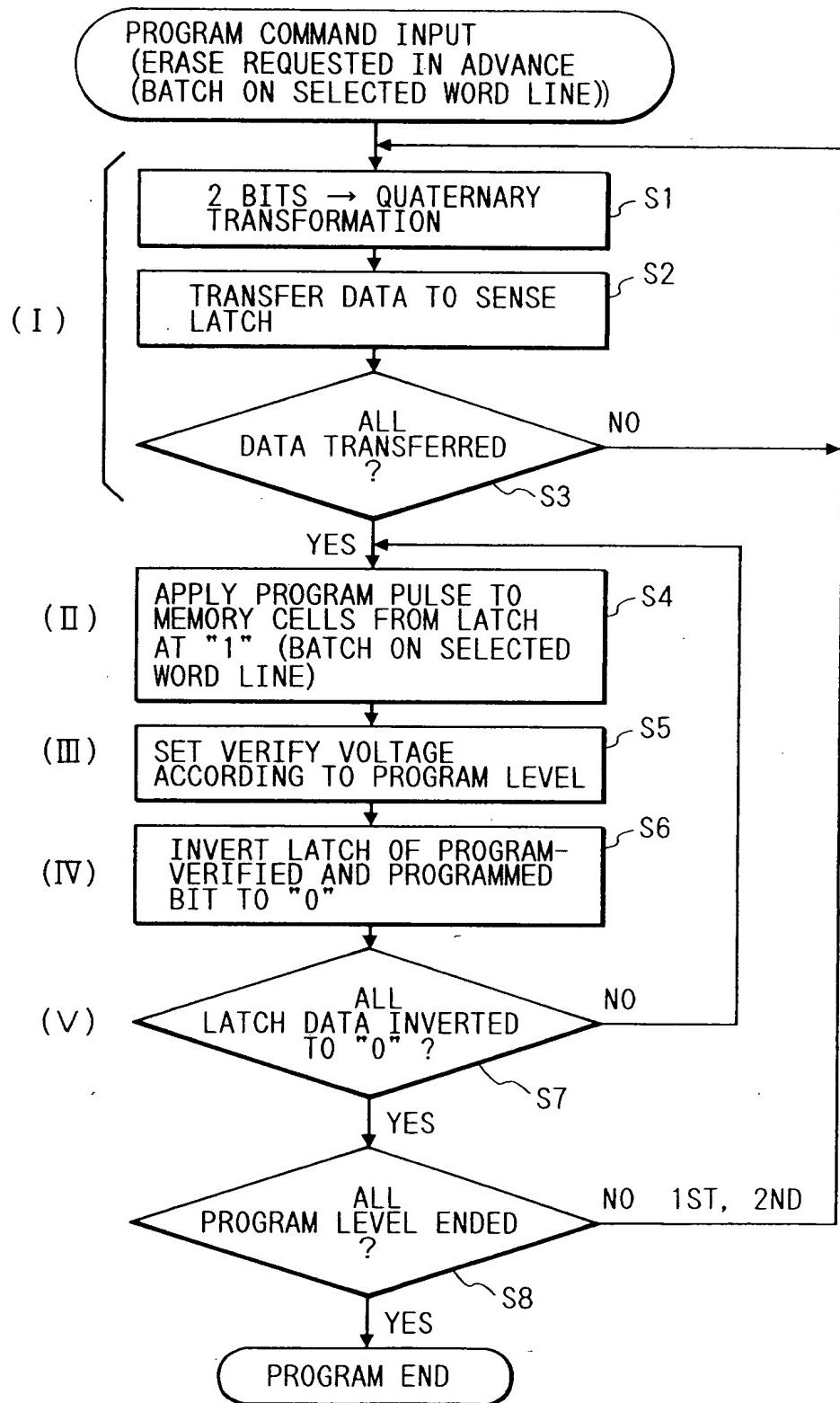


FIG. 6

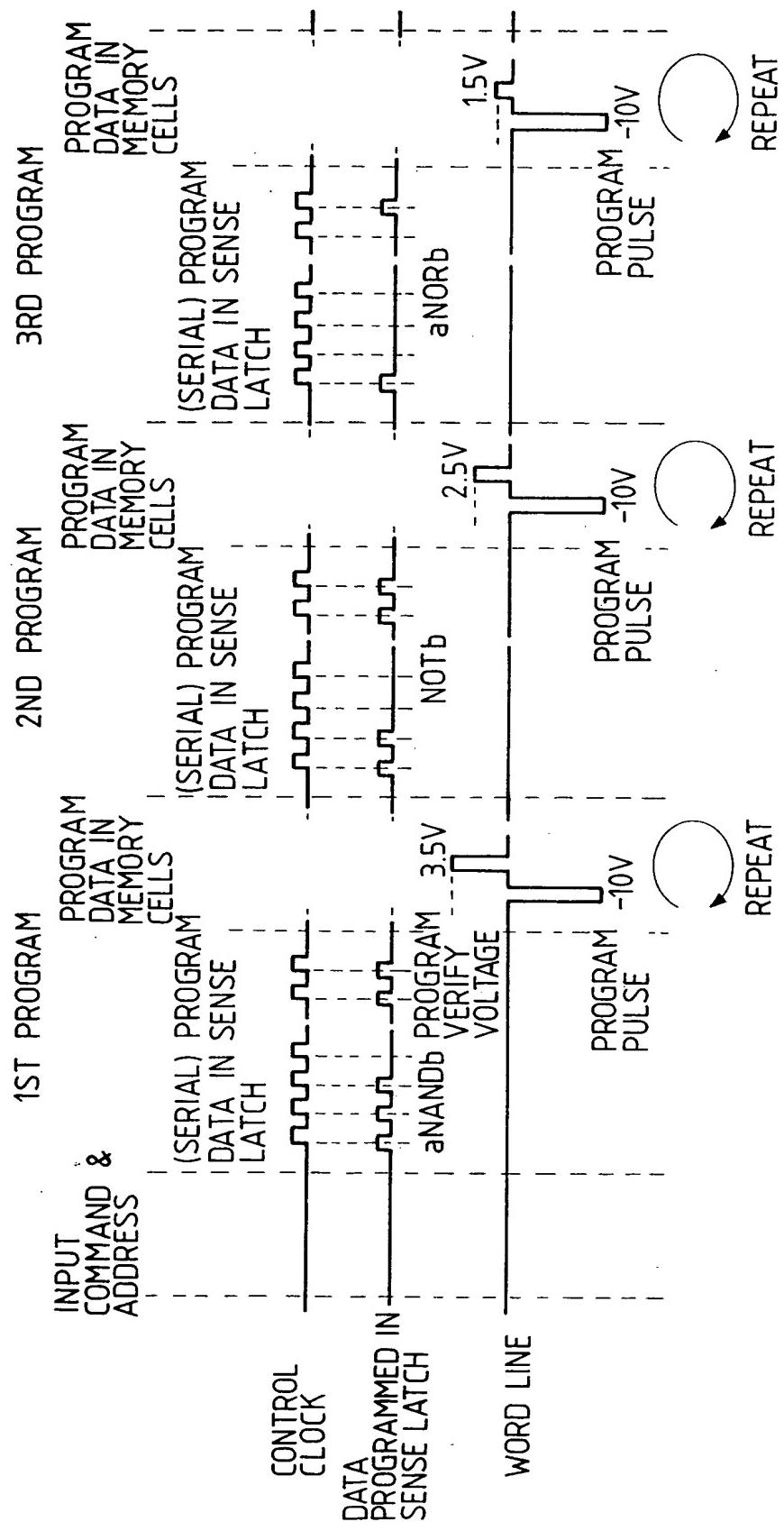
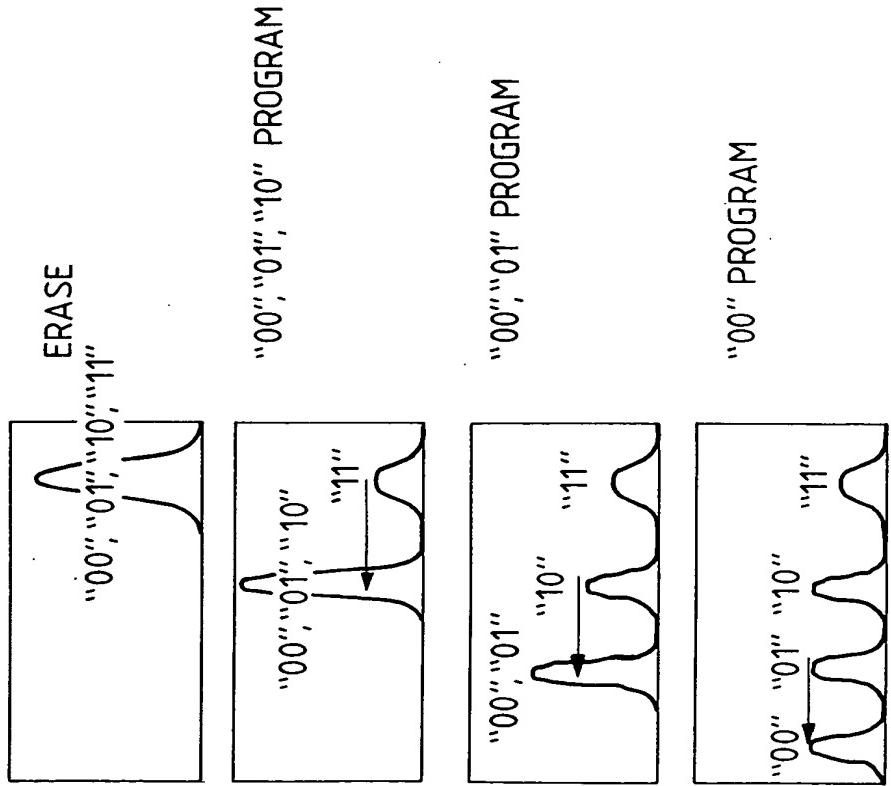
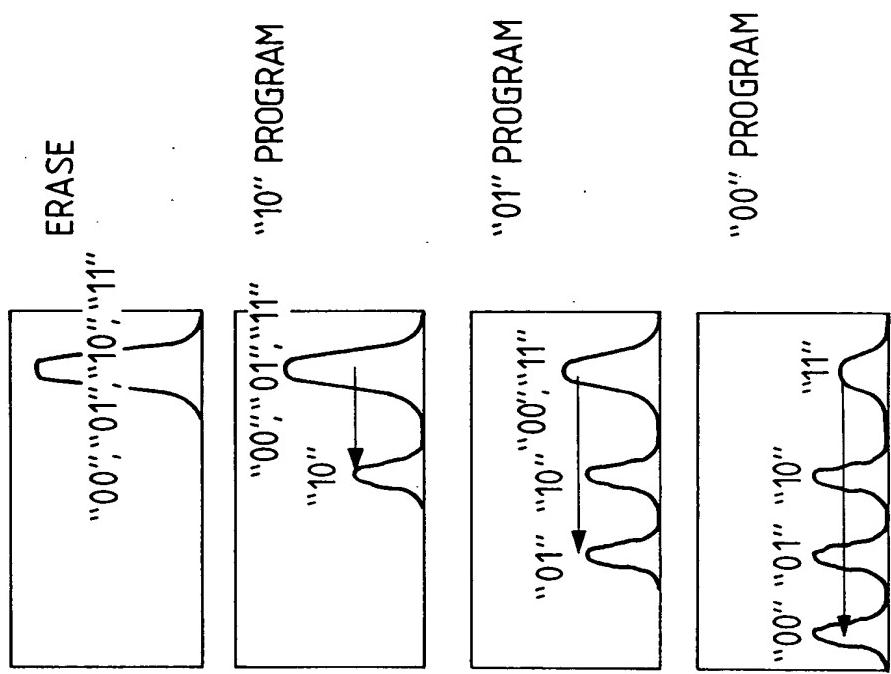


FIG. 7

(B)



(A)



1. BATCH OF PLURAL
LEVELS

2. EACH UNIT LEVEL

FIG. 8

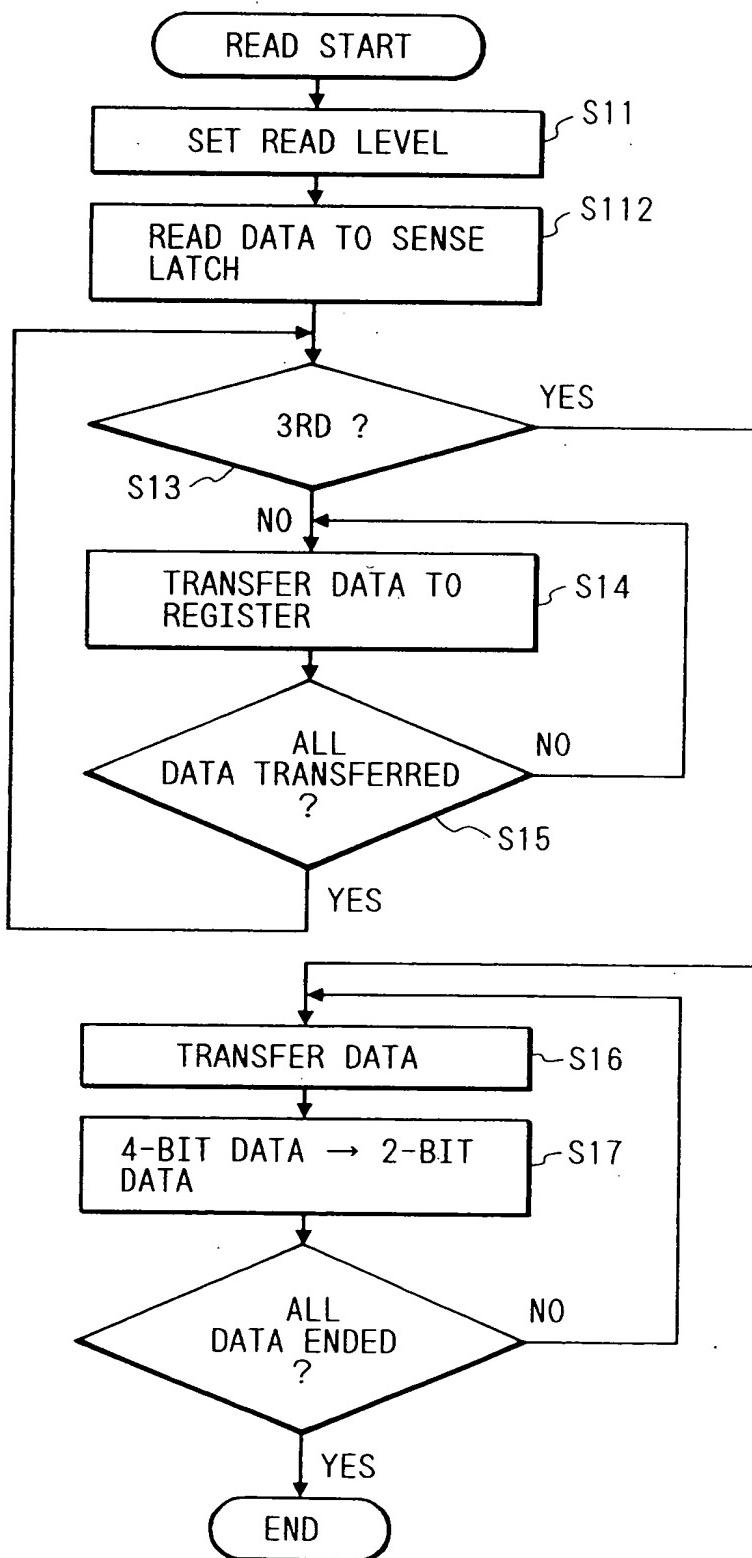


FIG. 9

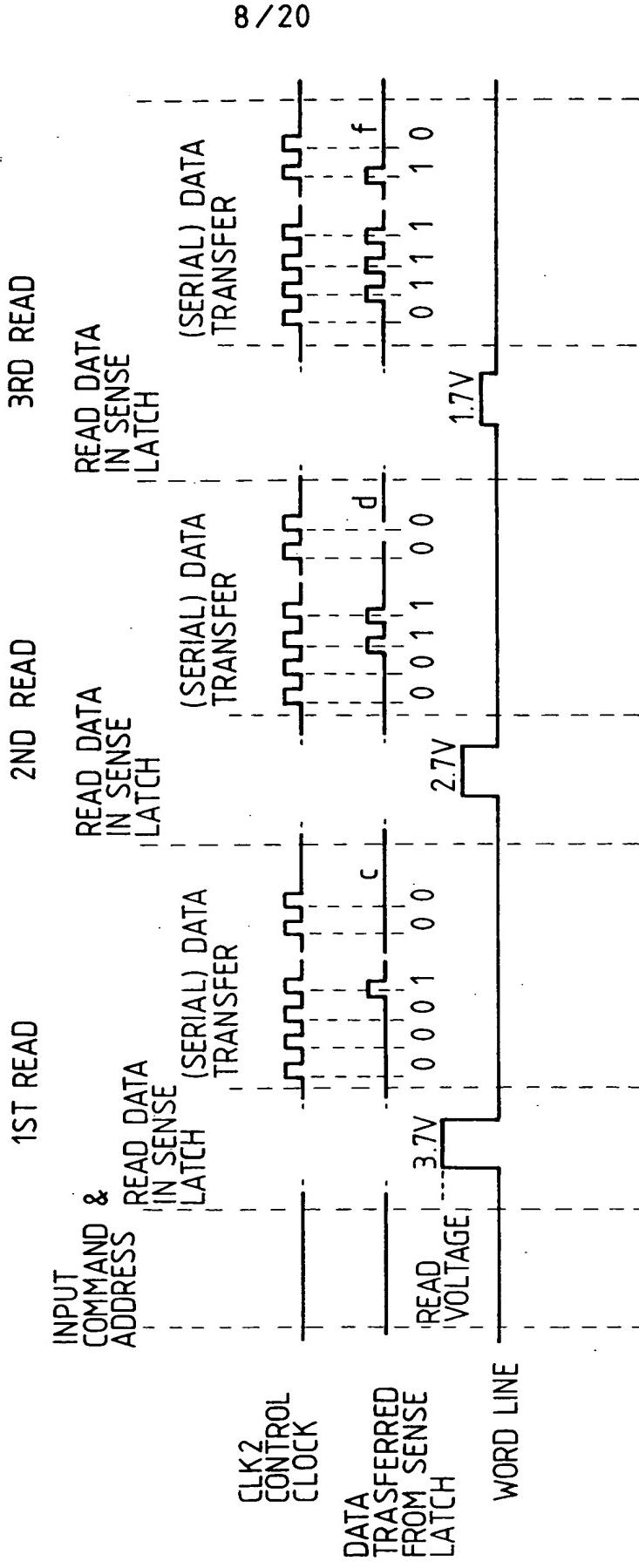


FIG. 10

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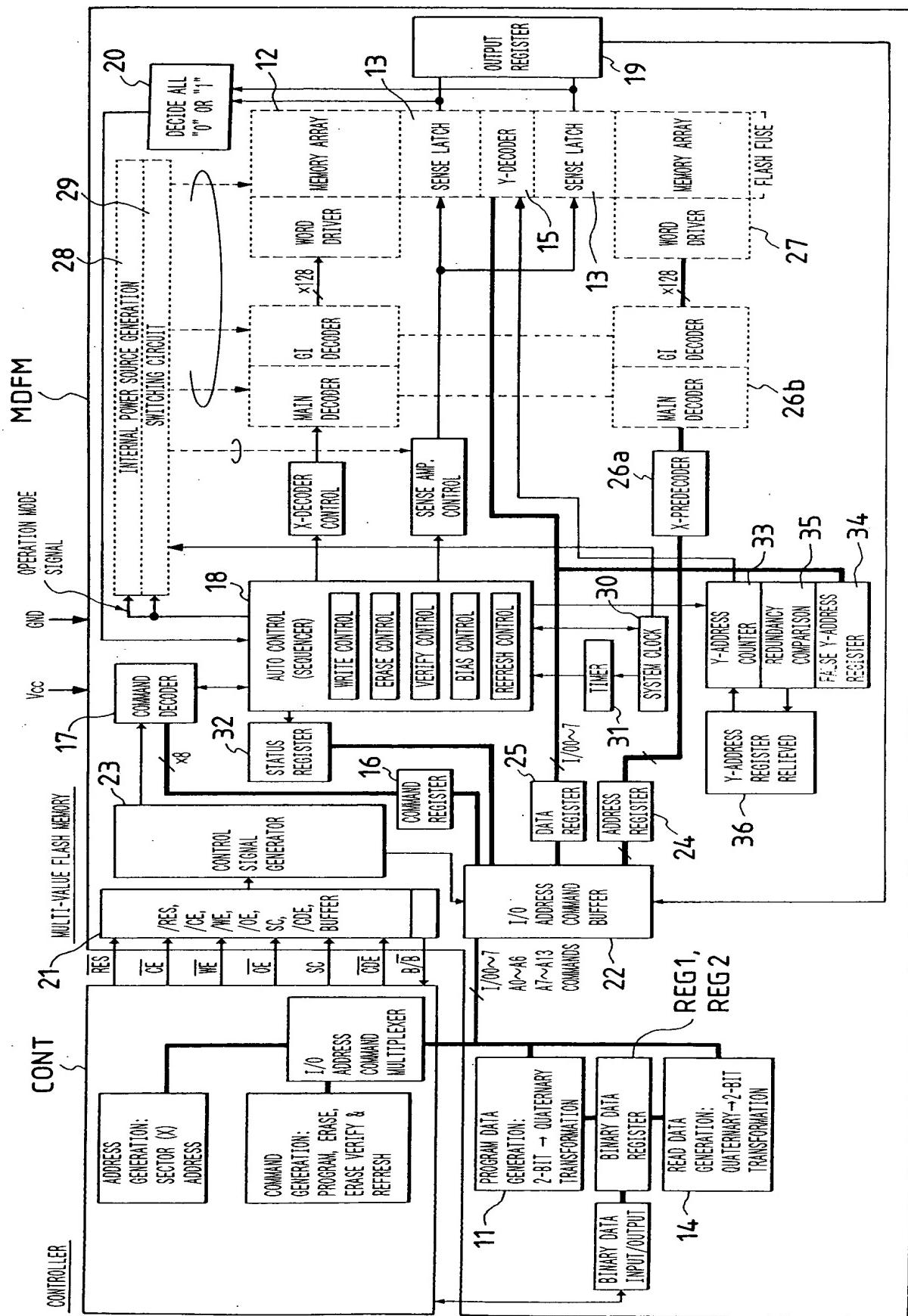


FIG. 11

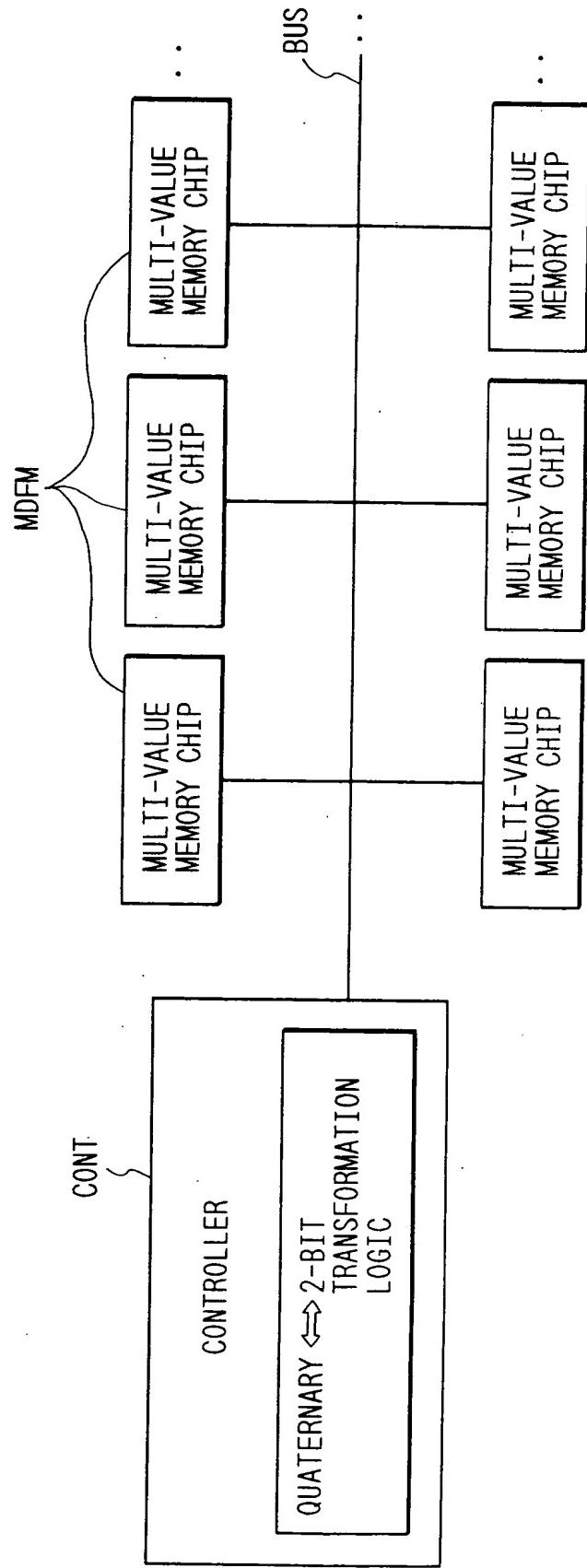
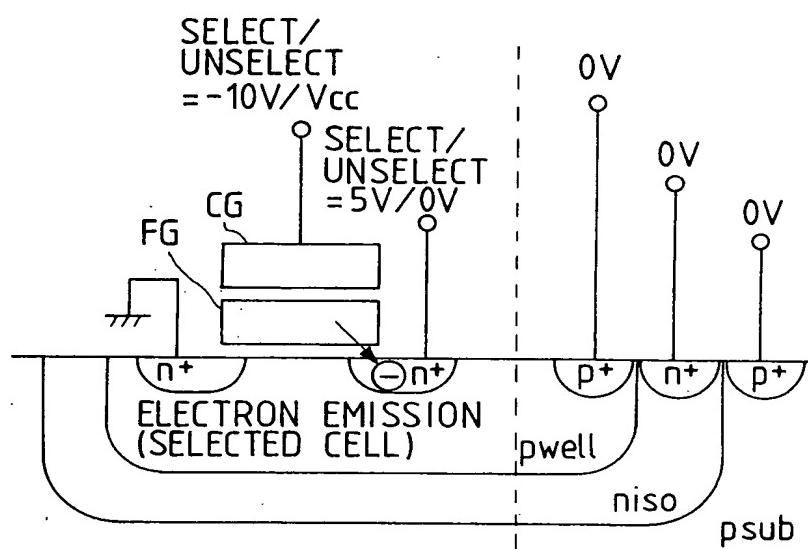
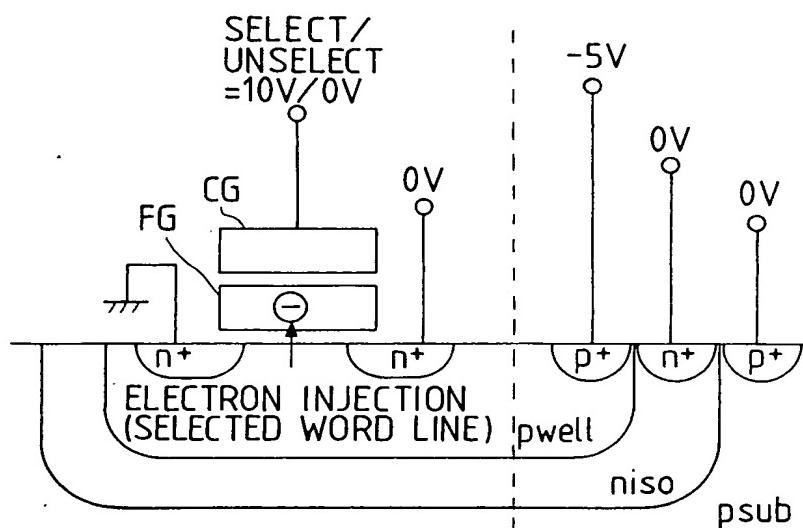


FIG. 12



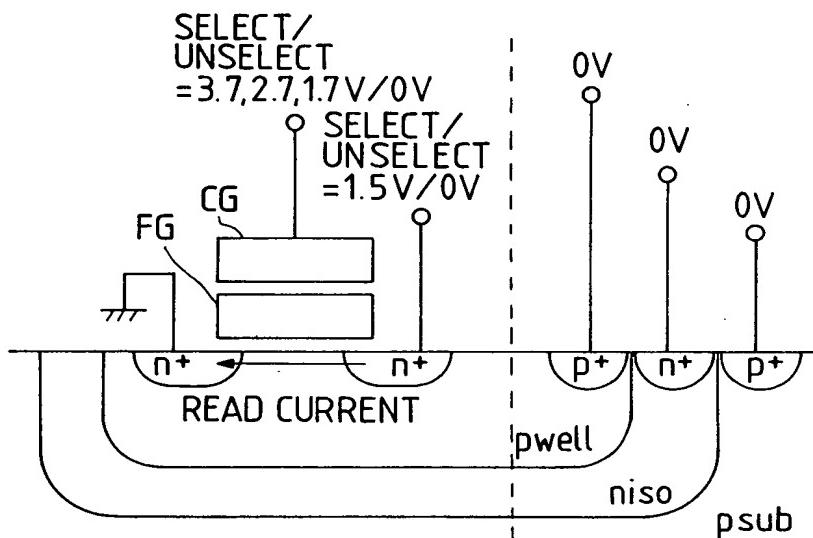
EXAMPLE OF APPLIED VOLTAGES
AT PROGRAMMING TIME

FIG. 13



EXAMPLE OF APPLIED VOLTAGES
AT ERASING TIME

FIG. 14



EXAMPLE OF APPLIED VOLTAGES
AT READING TIME

FIG. 15

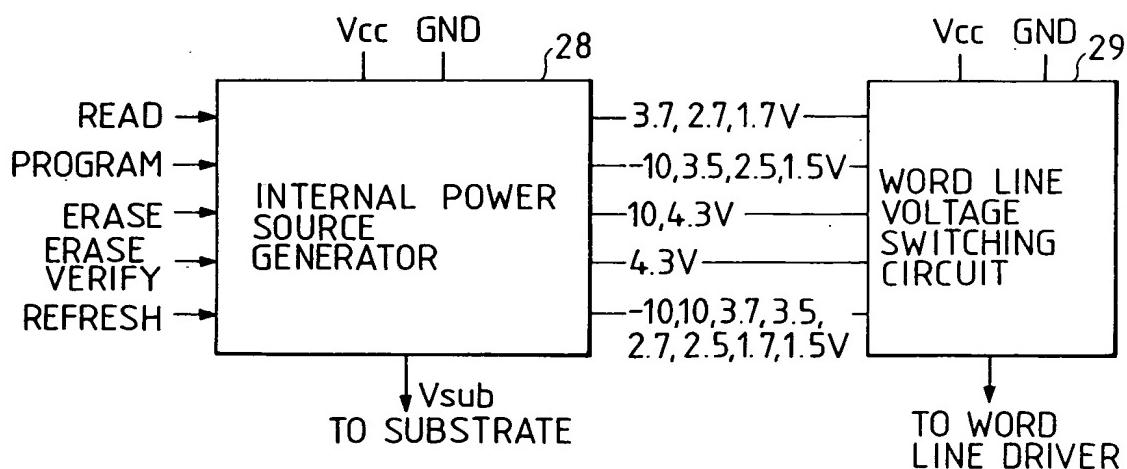


FIG. 16

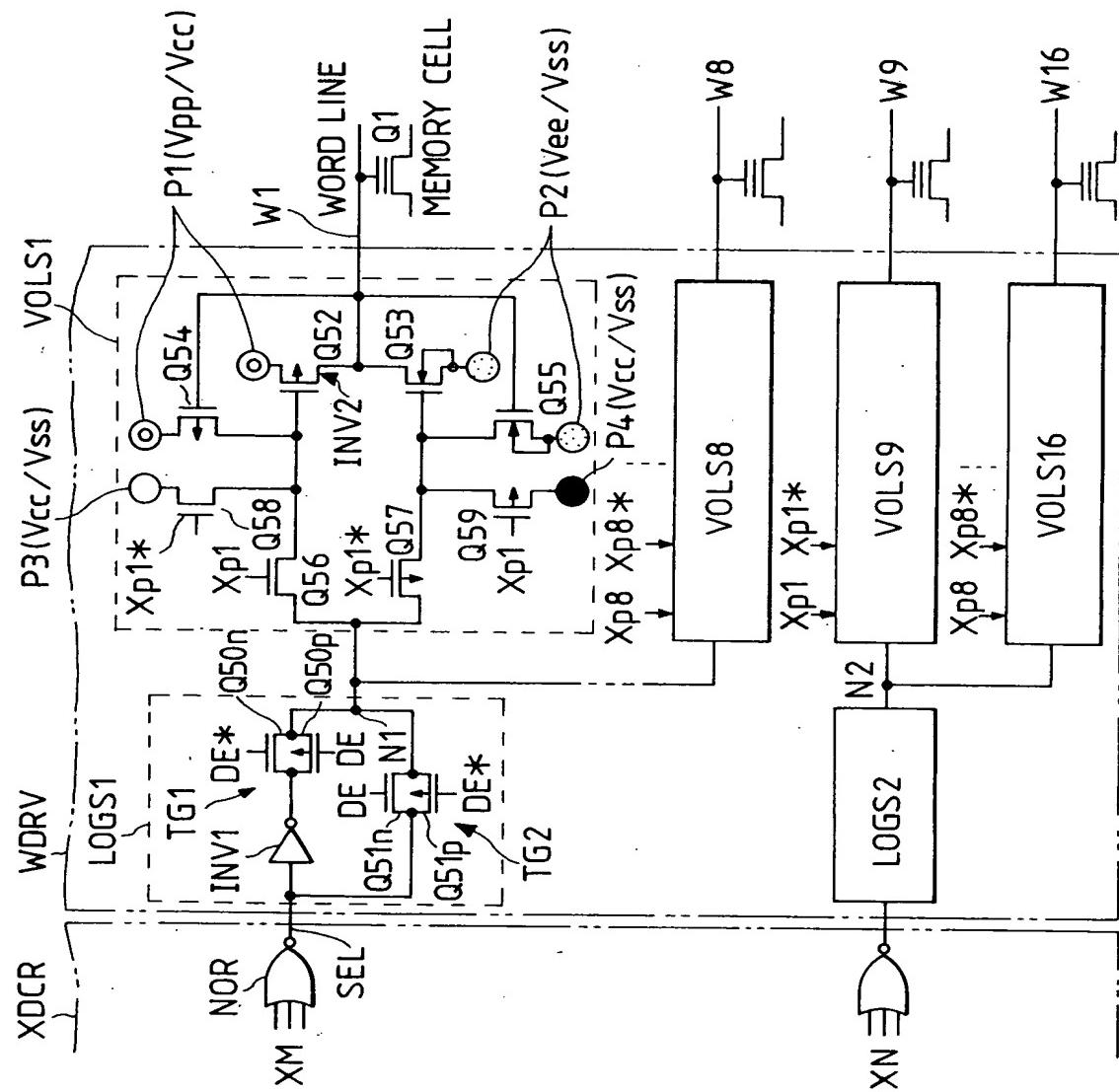


FIG. 17

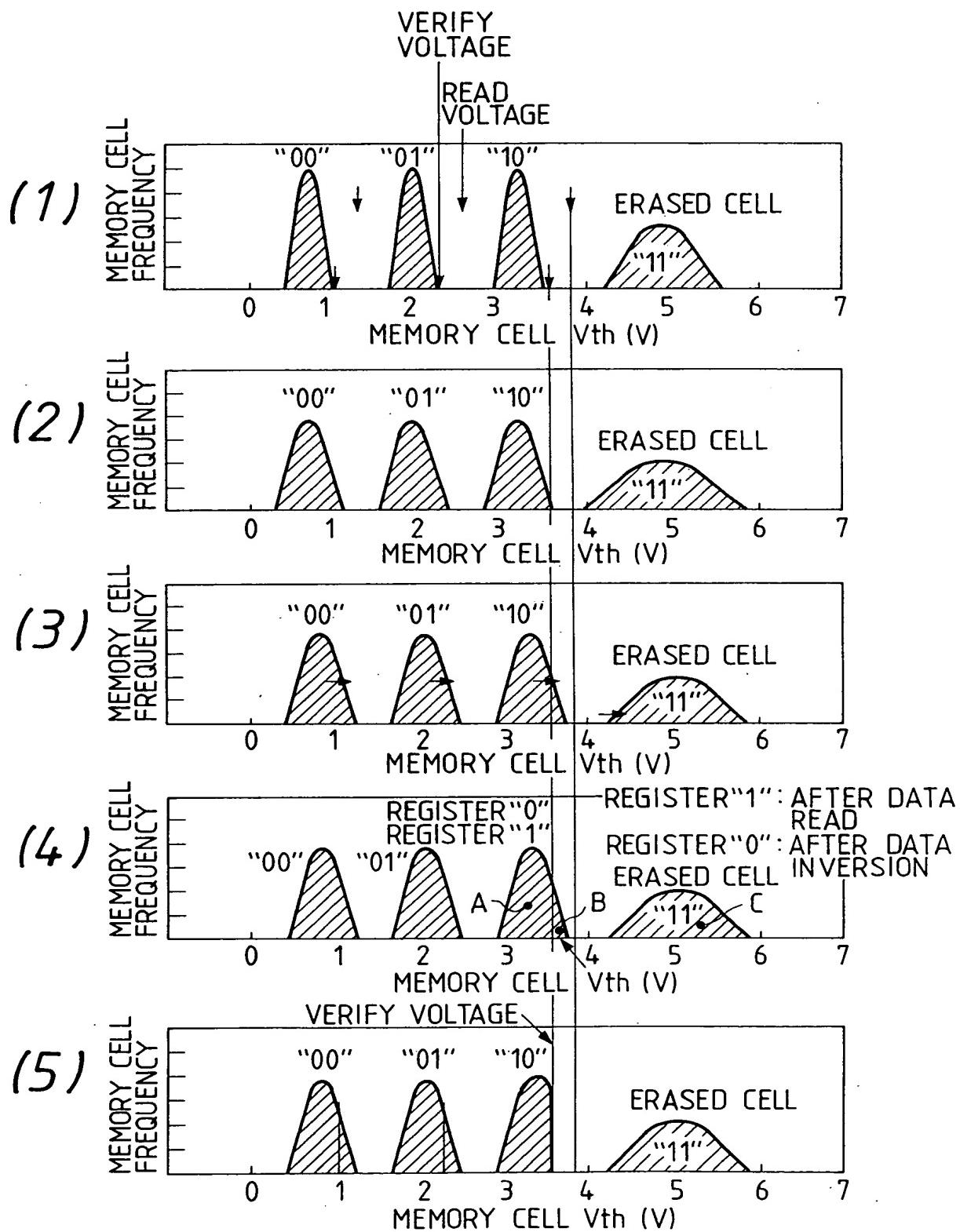


FIG. 18

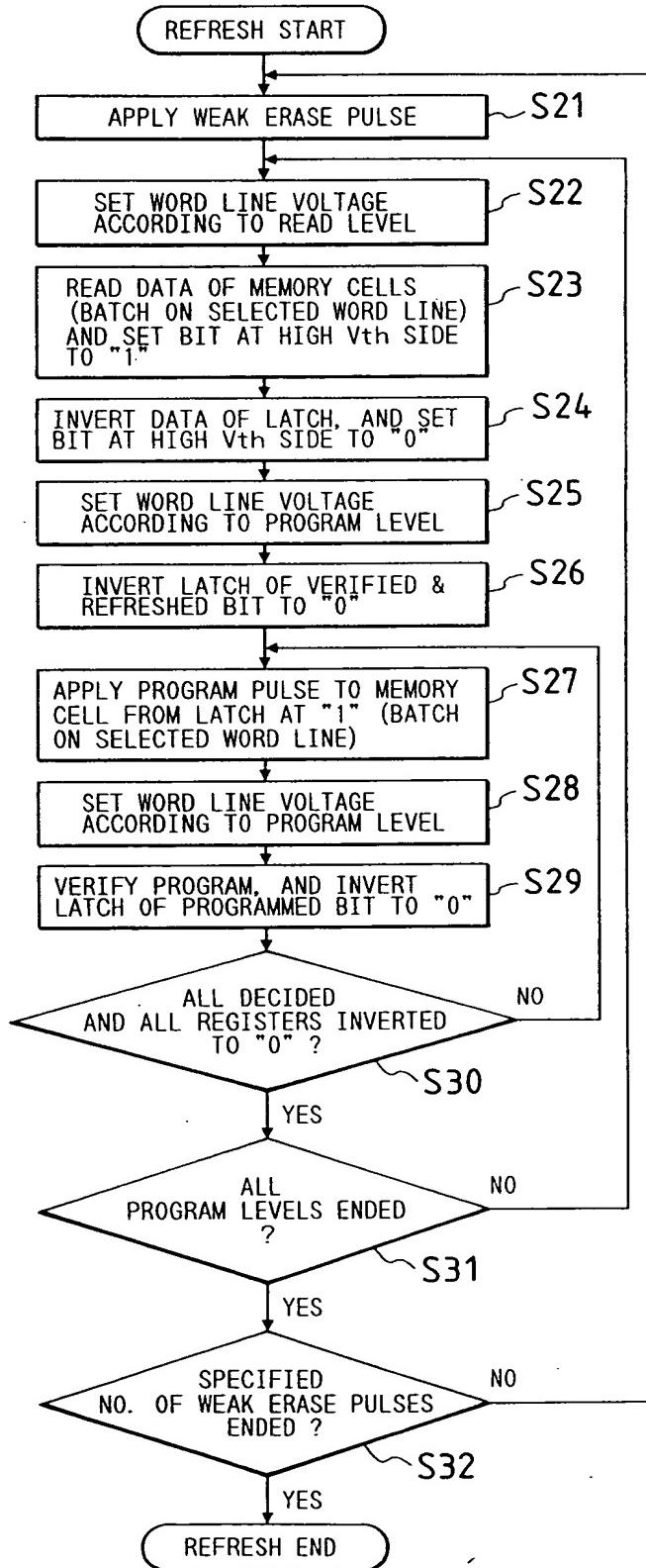


FIG. 19

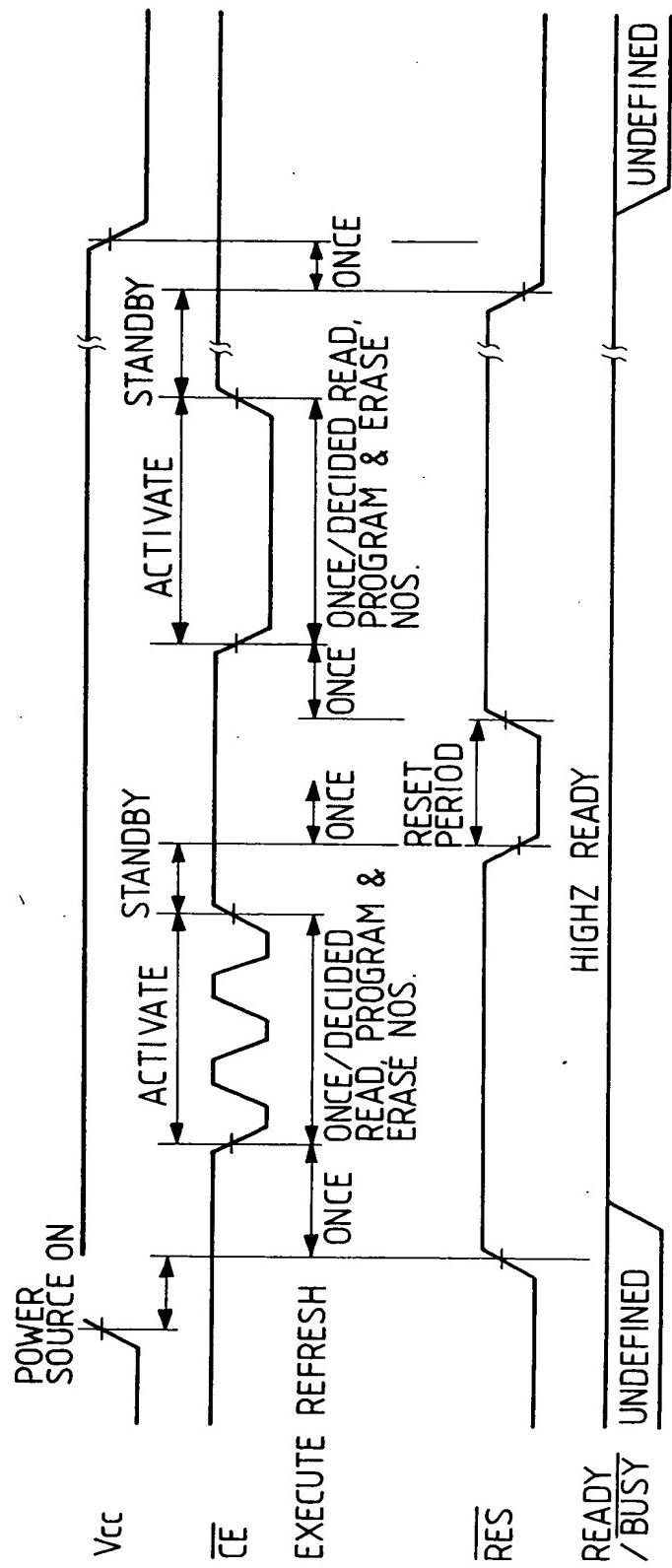


FIG. 20

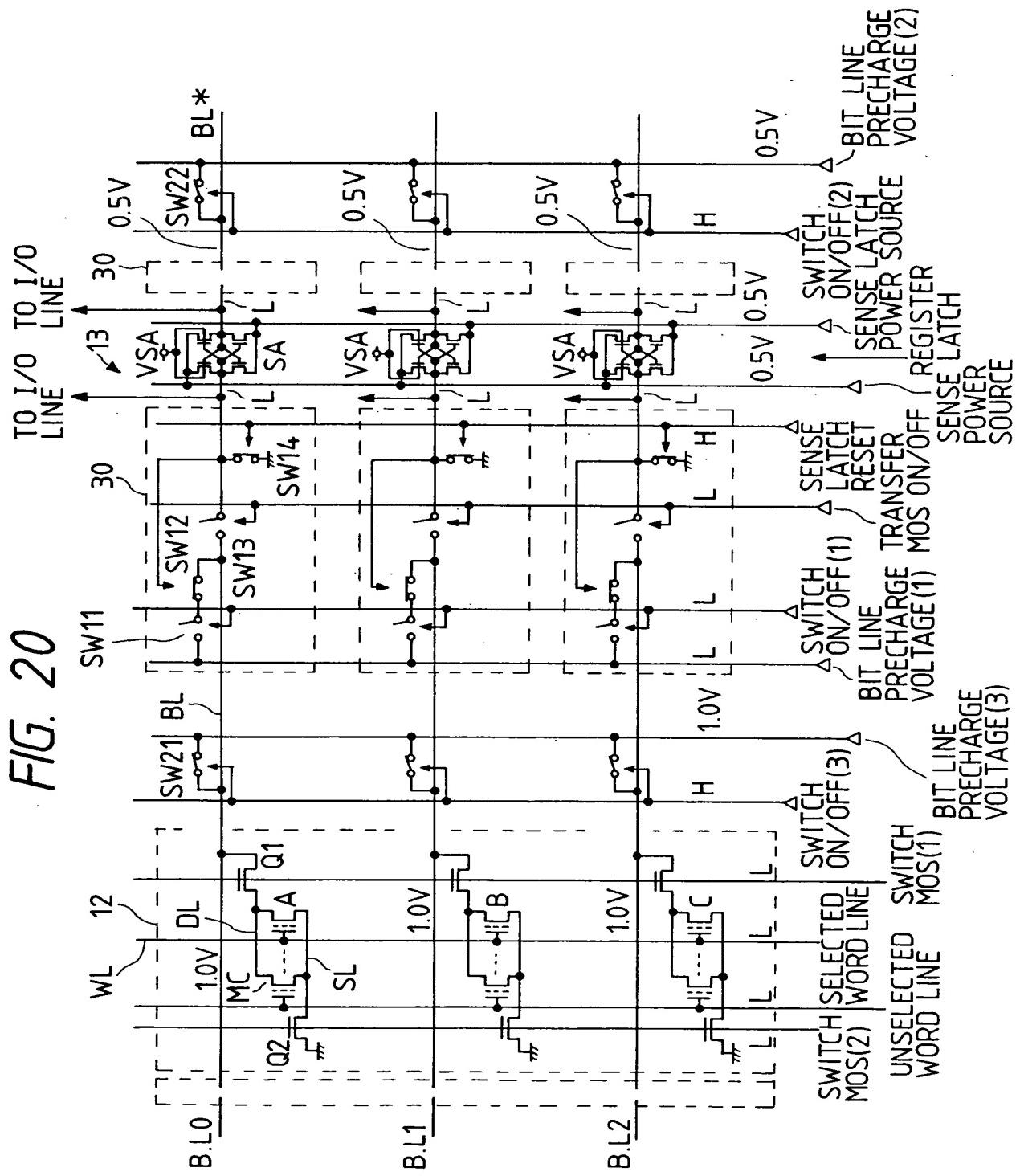


FIG. 21

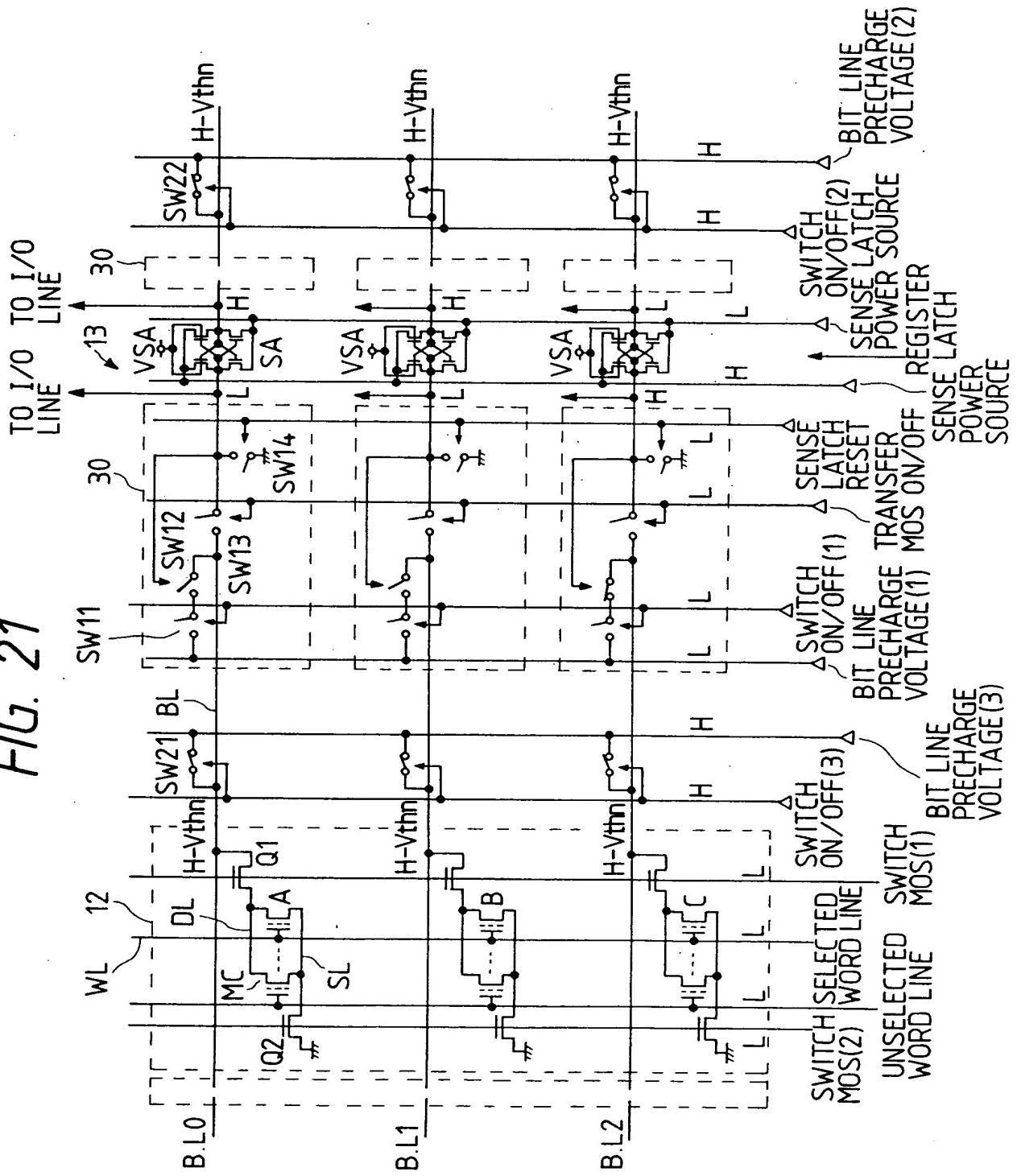


FIG. 22

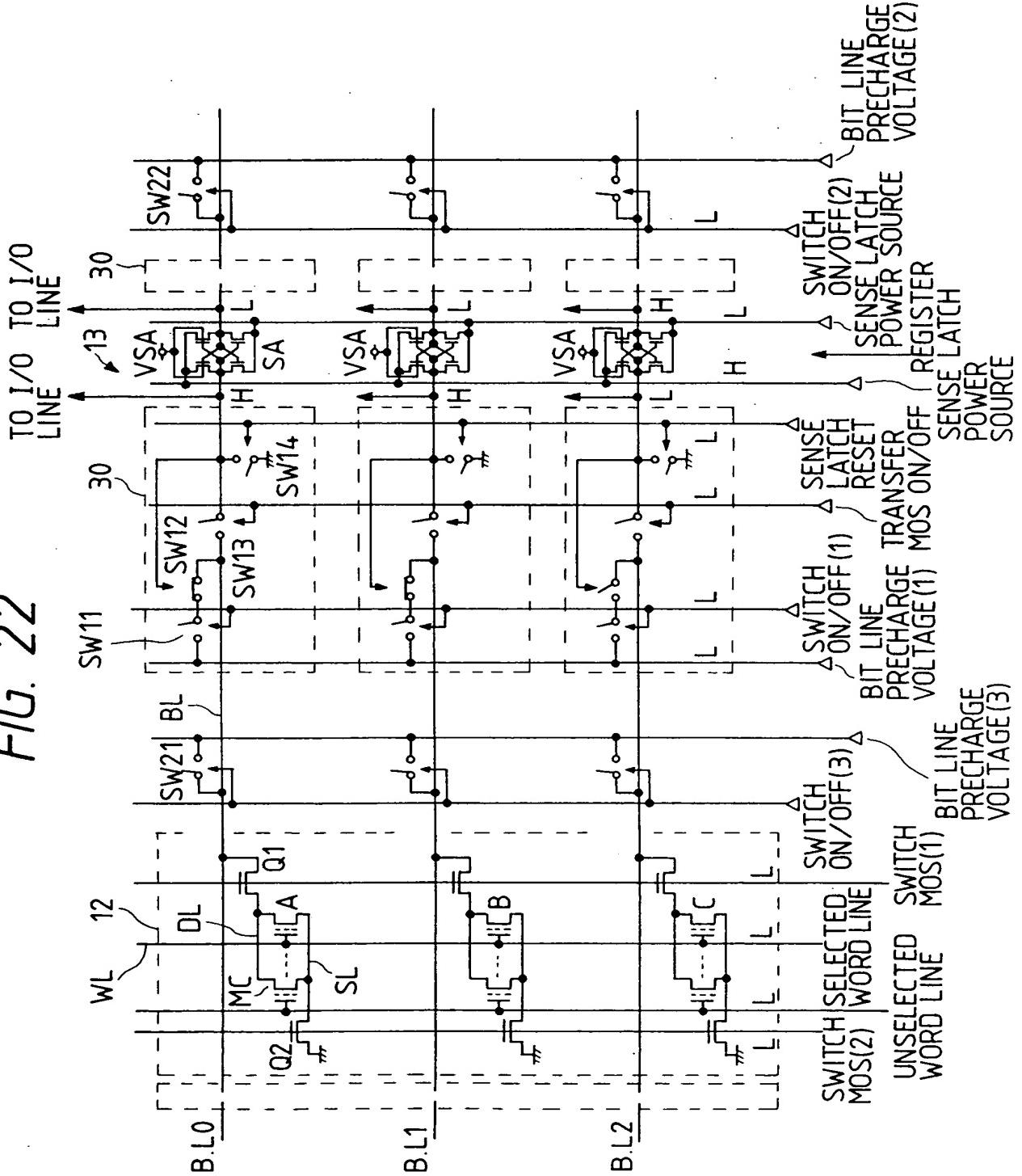


FIG. 23

